CC-10 (Analog Systems and Applications)

Two Port Devices

Short Type Question (2):

1. Draw the circuit diagram of a full wave rectifier with a filter.

2. What is the difference of ordinary diode and Zener diode?

3. What is dynamic resistance? Why the dynamic resistance of an ideal Zener diode is zero but the d.c. resistance is not so?

4. What are the transition capacitance and diffusion capacitance of a p-n junction diode?

5. What is peak inverse voltage in connection with a diode rectifier? What is its value in case of half wave and full wave rectifier with centre-tapped transformer?

6. Distinguish between full wave and half wave rectifier.

7. Derive the expression of the percentage regulation for a half wave, full wave and bridge rectifier circuit, each employing the same capacitor filter and the same load resistance.

Long Type Questions:

1. With the help of circuit diagram explain the operation of a Zener diode as a voltage regulator.(3)

2. Explain the avalanche and Zener breakdown mechanism. (3)

3. A full wave rectifier uses two semiconductor diodes with forward resistance R_f. Find the rectification efficiency when the load R_L is derive by the rectifier. Draw the wave form of the output voltage.

4. Explain the role of a type L-C filter in a rectifier circuit. (3)

5. Define ripple factor and rectification efficiency for a rectifier. Considering these two quantities Show that a full wave rectifier performs better than a half wave rectifier. (2+4)

6. Explain the working principle of light emitting diode. (3)

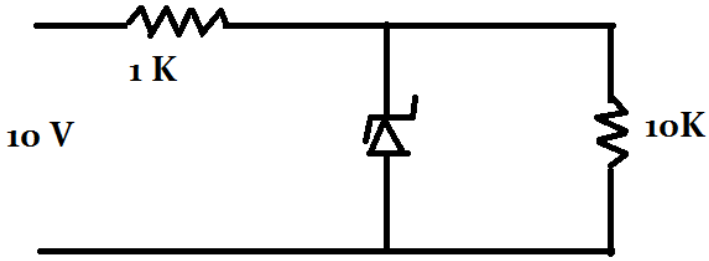
7. Explain the working principle of (i) LED, (ii) Solar cell and (iii) photodiode.

Numerical Problems:

1. What is the maximum possible current through a 5.6 V, 400 mW Zener diode? (1)

2. What are the current flowing through 1 K, 10 K resistor and the Zener in the circuit shown? Assume the Zener to be ideal and the breakdown voltage 6 volt. How will you answer the change if 10 K resistor is replaced by 500 resistors? What is the voltage across

the Zener now? Assume that the current through the Zener is zero if the voltage across it is less than the breakdown voltage.



3. A 12 volt zener diode is connected in series with a resistance 150 and a load resistance of 1 K is connected across the zener diode. The minimum Zener current is nearly zero and maximum Zener current should not exceed 20 mA. Calculate the operating range of input voltage. (4)

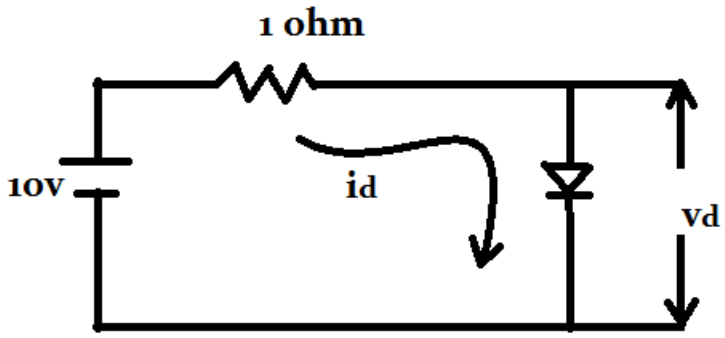
4. Prove that the maximum d.c. output power occurs in a half wave rectifier when the load resistance is equal to diode resistance.

5. In the given circuit current through diode i_d define as

$i_d = v_d{}^2 + v_d$ when $v_d > 0$

$= 0$ when v_d 0

v_d is the voltage drop across the diode. Find the value of v_d.



Transistor

Short Type Question (2):

1. Draw the output characteristic curve of a transistor in CE mode and lebel different portion of the curve.

2. What is emitter follower circuit.

3. What do you mean and of a transistor.

4. Find the relation between I_C and I_E in the active region.

5. Why the emitter region is heavily doped than the base region?

6. What is early effect? How can it account for CB input characteristic?

7. Show the different current component of a p-n-p transistor when the emitter junction is forward bias and collector junction is reverse bias.

8. Show the energy variation in the conduction band for the unbiased and biased transistor.

9. What are the factors for the shift of Q point of a transistor amplifier.

Long type Question:

1. Explain Q point and load line of a transistor. (3)

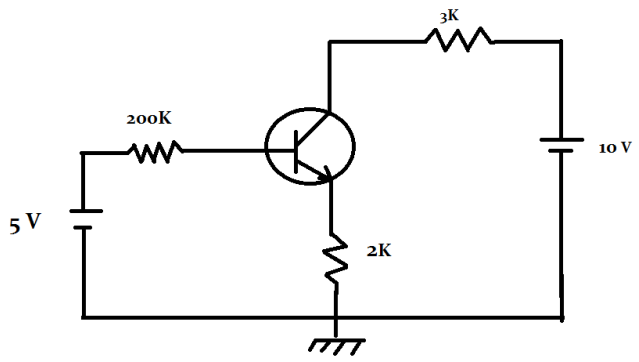
2. Sketch the output characteristics of a CB mode p-n-p transistor and explain its active region. (2+3)

3. Define and show that $I_C =$ I_B in the active region indicating why the relation is approximate.

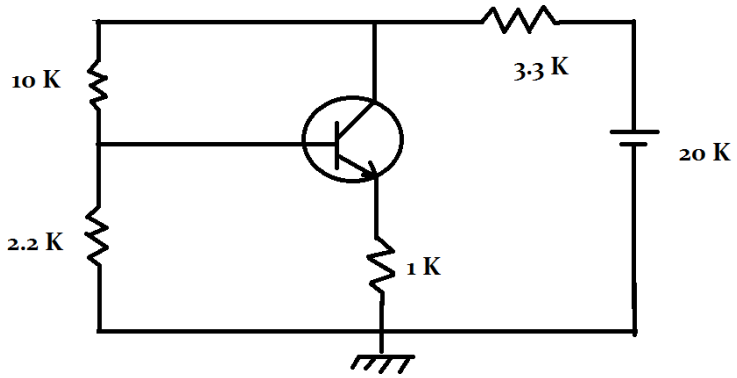
4. Draw the circuit diagram for the study of static characteristic of a n-p-n transistor operating in CE/CB mode. Sketch two important characteristics of these mode and briefly explain.

Numerical Problems:

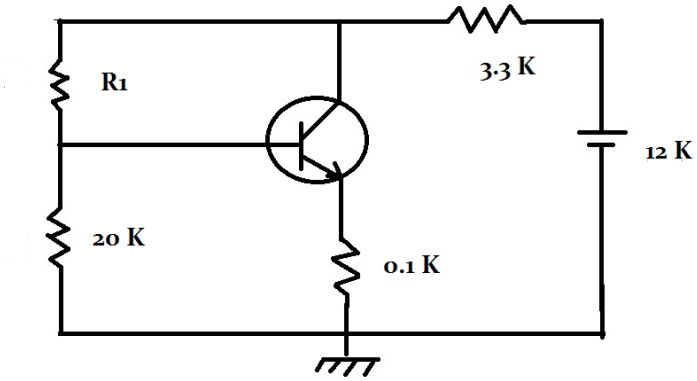
1. A Si transistor with = 100, $V_{BE} = 0.7$ V, $I_{CO} = 20$ nA is shown in the figure below. Find the values of I_C, I_E, I_B, V_{CE}. (3)



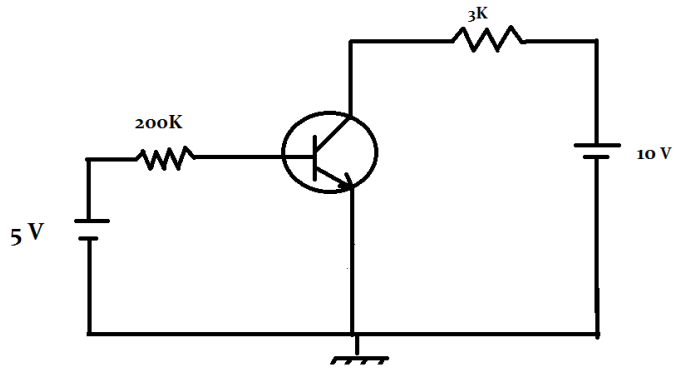
2. In the following figure find the Q point if = 150. (3)



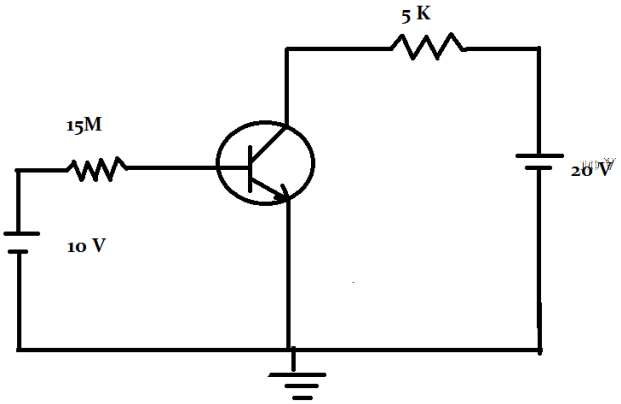
3. In the following circuit = 0.98, V_{BE} = 0.7 V, I_{CO} is negligible. For an emitter current I_E = 2 mA, Calculate I_C, I_B, R_1.



4. (a) Find the transistor current IC, IB, IE in the circuit below. Assume = 100, V_{BE} = 0.7 V, I_{CO} = 20 nA. (2)

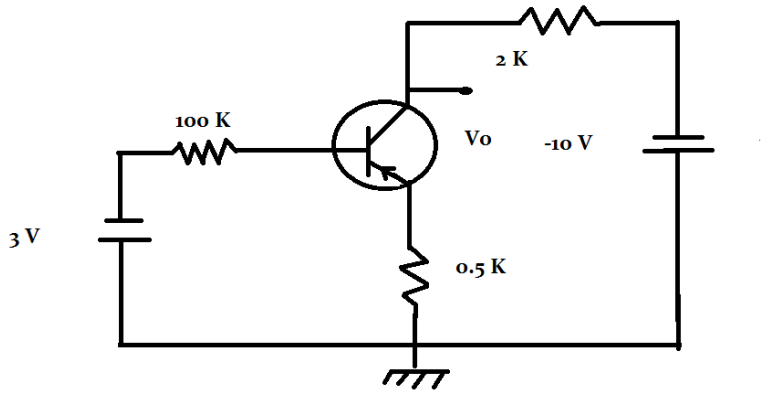


5. For a transistor in CE configuration shown in the figure, it is found that for a fixed base current 30 µA, collector current changes from 3.5 mA to 3.7 mAwhen the collector emitter voltage changes from 7.5V to 12.5V. Calculate the value and V_{CE} if = 125, V_{BE} = 0.7 V.



8. A transistor if connected in ce configuration in which collector supply 8 V and the voltage drop across the resistance 800 ohm connected in the collector circuit is 0.5 V. If = 0.96 determine collector emitter voltage and base current.

9. Find whether the transistor is working in active, saturation or cut off region and also find the value of V_o. Given = 100, V_{BE} = 0.7, V_{CESat} = 0.2 V



FET

Short type Question:

1. Why we call FET a voltage controlled device but BJT a current controlled device.

2. How a FET is used as a voltage variable resistance?

3. Why MOS device is commercially more important than the JFET?

4. What is the difference between depletion and enhancement MOSFET?

5. Write down four difference between JFET and a BJT.

6. When the channel of a JFET is said to be pinched off?

7. Draw the static charecteristics of a common source n-channel FET and give corresponding circuit diagram.

8. Compare between E-MOSFET and D-MOSFET.

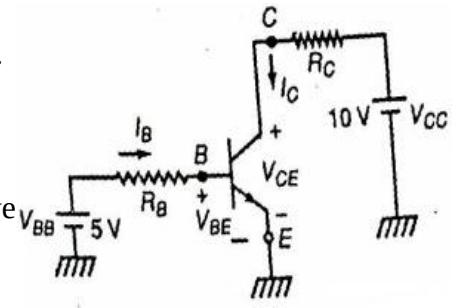
Long type question:

1. Explain the working of a p-channel enhancement MOSFET. (3)

2. What is the threshold voltage of enhancement MOSFET? What advantages does it contribute if V_T is of lower value? (1+2)

3. Sketch the basic structure of n channel depletion MOSFET. Draw the drain characteristicof this MOSFET. (3+2)

4. For a JFET write down the relationship between I_D and V_{GS}. Draw the nature of depletion region in an n-channel JFET (common source) at pinch off voltage. (1+2)



5. Draw the drain characteristic and transfer characteristic curve of an n-channel JFET and explain the nature of the curve. Define transcoductance of a JFET. (2+1)

Numerical Problems:

1. An n channel silicon JFET has channel half width a = 3 X 10^{-6} m and doping concentration $N_D = 10^{21}$ m^{-3}. Find the pinch voltage (given dielectric constant of silicon = 12).

2. An n channel JFET has I_{DSS} = 12 mA and pinch off voltage V_P = -4V. Find the drain current for V_{GS} = -2V. If the transconductance (g_m)of JFET at V_{GS} = 0 is 4 milliohm, find the pinch-off voltage.

Amplifiers

Short type Question:

1. Establish the relation $I_C = \beta I_B + (1 + \beta)I_{CBO}$ for CE transistor in active region.

2. Thermal noise in a CE circuit is much higher than that in a CB circuit Explain.

3. The value of α of a transistor is 0.98. If it changes by 0.5% what would be the corresponding percentage change in the value of β?

4. Explain the terms: (i) rating of a transistor (ii) thermal runway

5. What do you mean by the stability of bias point of a transistor?

6. Find the stability factor of a voltage divider type transistor biasing circuit using emitter resistance.

7. What are the sources of instability of Q-point?

8. Define the stability factors with respect to ICBO and β.

Long type question:

1. Show with a diagram the different current components in a p-n-p (or an n-p--n) transistor with emitter-base junction forward biased and collector-base junction reverse biased.

Define transistor α and β. How are they related?

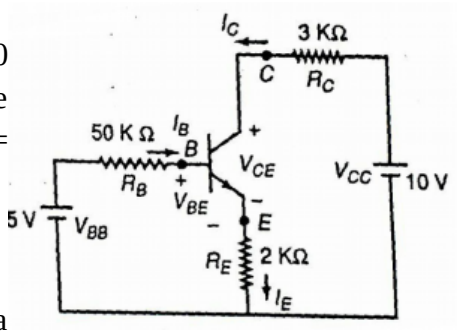
2. Draw the output characteristic curves of an n-p-n transistor in CE mode. Discuss about the different operating regions. Explain the nature of the curves. What is Early effect?

3. A transistor is connected in CE configuration in which collector supply is 8V and the voltage drop across a resistance 800Ω connected in the collector circuit is 0.5 V. If α = 0.96, determine (a) the collector-emitter voltage and (b) the base current.

4. Consider the adjacent circuit with R_B= 200 kΩ and R_C = 3 kΩ. (a) Find the transistor currents I_C, I_B and I_E. Assume a silicon transistor with β = 100, I_{CBO} = 20 nA, V_{BE} = 0.7 V. (b) Repeat the part (a) if a 2 kΩ resistor is added between the emitter and ground.

5. An n-p-n transistor is connected in CB mode and gives a reverse saturation current I_{CBO} = 12 μA. If α = 0.98, determine the base current and collector current for an emitter current of 2 mA.

6. The transistor in the adjacent Fig. has β = 100 and I_{CBO} = 20 nA. Calculate I_B, I_C, V_{CE} and hence decide in which region the transistor operates. Given $V_{BE,active}$ =0.7 V; $V_{BE,sat}$ = 0.8 V; $V_{CE,sat}$ = 0.2 V.



7. What do you mean by 'biasing of a transistor'? Explain why a transitor needs biasing. What is meant by 'stability of biasing'?

8. What do you mean by load line and Q-point of a transistor amplifier?

Explain the significance of load line. What are the criteria for selecting the position of Q-point in an amplifier? (c) What are the factors that affect the bias stability of a transitor?

9. Draw a neat circuit diagram of a fixed bias arrangement applied to an n-p-n, transistor in CE mode. Why is it called fixed bias? Explain how you can find the Q-point of the circuit. What are the functions of the coupling capacitors? Discuss the stability of fixed biasing arrangement.

10. Draw a self bias circuit. Why is it so caned? Define bias curve. Explain how the bias curve is used to find the Q-point of the circuit. With suitable circuit diagram, discuss the operation of a voltage divider biasing circuit. Establish that a self bias is superior to fixed bias.